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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,728	NANJA, MURTHI	
	Examiner	Art Unit	
	ERIC CHANG	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,11-20 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,11-20 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-8, 11-20 and 22-26 are pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-2, 4-8, 11-20 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 7,111,179 to Girson et al., in view of U.S. Patent 6,230,313 to Callahan et al.

4. As to claim 1, Girson discloses an article comprising a machine-accessible medium having stored thereon instructions that, when executed by a machine, cause the machine to: obtain from a performance monitor runtime performance of a thread level utilization, wherein the runtime performance data is indicative of a set of execution characteristic of the thread including an IPC metric [32, 42], obtained from a timer interrupt in the performance monitor [30]; and based on the performance data, adjust an operating voltage or an operating frequency of the machine [col. 5, lines 16-33], wherein the operating voltage and operating frequency are nonzero [col. 6, lines 58-59].

Girson teaches the limitations of the claim but does not teach that the runtime performance data includes a memory references-per-cycle metric.

Callahan teaches that monitoring thread level runtime performance data of threads running on a machine, including instructions-per-cycle data [col. 6, lines 16-25]. Thus, Callahan teaches monitoring runtime performance data similar to that of Girson. Callahan further teaches that runtime performance data includes a memory references-per-cycle metric [col. 19, lines 16-22].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the memory references-per-cycle metric as taught by Callahan. One of ordinary skill in the art would have been motivated to do so that power can be saved through the monitoring of processor performance data.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of monitoring performance data. Moreover, the memory references-per-cycle metric means taught by Callahan would improve the flexibility of Girson because it allowed a variety of performance data to be used in determining runtime performance of threads.

5. As to claim 2, Girson discloses the performance monitor is a Performance Monitoring Unit (PMU) [28], and is part of a central processing unit (CPU) [4] within the machine [FIG. 1].

6. As to claim 4, Callahan discloses a plurality of counters for simultaneously measuring multiple different performance data [col. 19, lines 16-22].

7. As to claim 6, Girson discloses that in response to the runtime performance data, determining if the operating voltage and operating frequency should be adjusted upward or scaled down [col. 5, lines 16-33].

8. As to claim 7, Girson discloses comparing the performance data to determine a voltage value and a frequency value [48].

9. As to claim 8, Girson discloses obtaining a plurality of runtime performance data [col. 7, lines 62-67, and col. 8, lines 1-6]; and in response to the plurality of runtime performance data, adjusting the operating voltage and the operating frequency [col. 8, lines 48-66].

10. As to claim 11, Girson discloses operating the performance monitor in an operating system environment in communication with a platform hardware environment, and in communication with an end user code, in a user mode [col. 2, lines 37-41].

11. As to claim 12, Girson discloses adjusting the operating voltage and the operating frequency [col. 5, lines 16-33].

12. As to claim 13, Girson discloses a method comprising: obtaining, from a performance monitor, runtime performance data indicative of a thread-level utilization, including an IPC metric [32, 42] for a central processing unit (CPU) having an operating voltage and an operating frequency [col. 2, lines 49-53]; in response to the runtime performance data, determining if either

the operating voltage or the operating frequency is at a desired value [col. 7, lines 62-67, and col. 8, lines 1-6]; and in response to the determination, adjusting the operating voltage or the operating frequency [col. 5, lines 16-33]. Callahan further teaches that runtime performance data includes a memory references-per-cycle metric [col. 19, lines 16-22].

13. As to claim 14, Girson discloses adjusting both the operating voltage and the operating frequency [col. 5, lines 16-33].

14. As to claim 15, Girson discloses adjusting the operating voltage and the operating frequency upward [col. 5, lines 16-33].

15. As to claim 16, Girson discloses adjusting the operating voltage and the operating frequency downward [col. 5, lines 16-33].

16. As to claim 17, Girson discloses the performance monitor [28] is a Performance Monitoring Unit (PMU) [28].

17. As to claims 19-20, Girson discloses comparing the performance data to determine a voltage value and a frequency value [48].

18. As to claim 22, Girson discloses a method comprising: a machine simultaneously monitoring runtime performance data [28]; and adjusting the operating voltage or the operating

frequency of the machine [col. 5, lines 16-33]. Callahan further teaches that runtime performance data includes multiple performance events where each performance event reflects a different thread level utilization of at least one application executing on the processor [col. 19, lines 16-22]; and based on the simultaneously monitored multiple performance events, obtaining multiple performance metrics indicating events per clock cycle of the at least one executing application [col. 6, lines 16-25].

19. As to claim 22, Callahan teaches that multiple performance metrics include instructions-per-cycle data and a memory references-per-cycle metric [col. 6, lines 16-25].

20. As to claim 23, Callahan discloses simultaneously measuring multiple different performance data [col. 19, lines 16-22].

21. As to claim 24, Callahan discloses simultaneously measuring multiple different performance data from different applications executing on the processor [col. 19, lines 16-22].

22. As to claim 25, Callahan discloses the machine simultaneously monitoring multiple performance events from different applications executing on the processor [col. 12, lines 7-25].

23. As to claim 26, Girson discloses using a different counter to monitor each performance event [col. 7, lines 4-8].

24. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 7,111,179 to Girson et al., in view of U.S. Patent 6,230,313 to Callahan et al., and in further view of U.S. Patent 6,233,690 to Choi, et al.

25. As to claim 5, Girson and Callahan teach the limitations of the claim, including monitoring performance data indicative of thread-level utilization, but does not teach that additional runtime performance data includes cache misses and other data dependency stalls.

Choi teaches that a computer can have its voltage or frequency adjusted due to the monitoring of performance data [col. 1, lines 11-45]. Thus, Choi teaches a performance-based voltage and frequency adjustment similar to that of Girson and Callahan. Choi further teaches that the runtime performance data is selected from the group consisting of instruction cache misses, data cache misses, instructions executed, stalls due to data dependency, and data cache write-backs [col. 2, lines 62-67, and col. 3, lines 1-10]. Other stall conditions well known in the art comprise branches executed, branch mis-predicts, instruction translation look-up buffer TLB misses and data translation look-up buffer TLB misses.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ additional runtime performance data as taught by Choi. One of ordinary skill in the art would have been motivated to do so that power can be saved through the monitoring of processor performance data.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of adjusting processor voltage or frequency due to the monitoring of performance data. Moreover, the additional runtime

performance data means taught by Choi would improve the efficiency of Girson and Callahan because it allowed for power-saving during long latency machine stalls [col. 2, lines 62-64].

26. As to claim 18, Choi discloses the runtime performance data is selected from the group consisting of instruction cache misses, data cache misses, instructions executed, branches executed, branch mis-predicts, instruction translation look-up buffer misses, data translation look-up buffer misses, stalls due to data dependency, and data cache write-backs [col. 2, lines 62-67, and col. 3, lines 1-10].

Response to Arguments

27. Applicant's arguments with respect to claims 1-2, 4-8, 11-20 and 22-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC CHANG whose telephone number is (571)272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eric Chang/
Examiner, Art Unit 2116

September 11, 2009

/Thomas Lee/
Supervisory Patent Examiner, Art Unit 2115